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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,011	09/10/1999	HERMAN LEE BLACKMON	RO999-080	3617

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EXAMINER

VITAL, PIERRE M

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/394,011	BLACKMON ET AL.
Examiner	Art Unit	
Pierre M. Vital	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 10 September 1999.

2a) This action is FINAL.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-21 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 10 September 1999 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.

4) Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

## DETAILED ACTION

### ***Specification***

1. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: "performance inlcud" on page 3, line 8; "command of each of type", page 7, line 11, etc.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
3. Claims 4-7 recite the limitation "said bus network" in the claims. There is insufficient antecedent basis for this limitation in the claim. There was no previous mention of "a bus network" in the claims.
4. Claim 17 recites the limitation "said determinations" in line 7. There is insufficient antecedent basis for this limitation in the claim. It is not clear why "all of the received address determinations" are being passed along with "a single memory command".
5. Claims 16 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation “said step of executing sequential valid commands of the same command type further *continues* a valid memory command of said command type is no longer available”. It is not clear what applicant means by this claim language since it does not clearly or specifically point out how or when the “executing step” is continued.

Claim 19 recites the limitation “said *plurality of bus units interconnected* on a bus network and said *plurality of bus units*”. It is not clear what applicant means by this claim language. As such, this limitation has not been treated on merits.

Claim 19 recites the limitation “at least one memory subsystem connected to said plurality of bus units *on a first bus*”. It is not clear what applicant means by this claim language. However, Examiner would interpret the claim language as meaning that “at least one memory subsystem connected on a first bus of said plurality of bus units”.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application

being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Stracovsky et al (US6,385,708).

As per claim 19, Stracovsky discloses a computer processing system comprising a plurality of bus units [Fig. 1A, elements 106]; said bus units comprising at least one computer processor [col. 6, line 2]; at least one I/O device [Fig. 1A, element 108]; at least one memory cache system connected to said at least one computer processor [col. 10, lines 28-30]; said memory commands categorized into types [col. 6, lines 30-43; col. 8, lines 22-24]; (b) at least one memory subsystem connected to said plurality of bus units on a first bus, said memory subsystem responsive to said memory commands [col. 6, lines 1-19]; and further comprising (i) a memory controller connected to a command interface functionally connected to said first bus [col. 6, lines 1-5, Fig. 1A, elements 104, 110, 106]; (ii) a plurality of memory chips configured into memory banks ; said memory chips architected into memory cards attached to at least one memory bus [col. 7, lines 35-38]; (iii) a plurality of command FIFO queues, each of said command FIFO queues associated with one of said command types into which said memory commands are categorized [Fig. 10, elements 1020, 1022]; (iv) a plurality of comparison logic circuits, each of said plurality of comparison logic circuits associated with each of said plurality of command FIFO queues to determine which memory command types have the least memory cycle performance penalty [col. 20, lines 12-30]; (v) an

arbitration logic circuit to output said memory commands of said determined command type having said least memory cycle performance penalty to said plurality of memory chips [col. 19, lines 2-34; col. 20, lines 31-50].

As per claim 20, Stracovsky discloses said comparison logic circuit further determines the oldest of said memory commands in each of said plurality of command FIFO queues [col. 19, lines 65-67].

#### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al (US6,385,708) and Harriman et al (US6,088,772).

As per claim 1, Stracovsky discloses a method for processing commands in a computer memory subsystem comprising (a) receiving a plurality of commands on a bus connected to said memory subsystem [col. 6, lines 1-19]; (b) categorizing said received commands into command types [col. 6, lines 30-43; col. 8, lines 22-24]; (c) determining memory cycle performance penalties of said categorized commands [col. 3, lines 2-11]; (d) reordering said categorized commands so that said categorized commands having

the least memory cycle performance penalty are selected for execution [col. 3, lines 7-11].

However, Stracovsky does not specifically teach (e) determining if said reordered commands are valid; (f) arbitrating said valid commands (g) executing sequential valid commands of the same command type as recited in the claim.

Harriman discloses (e) determining if said reordered commands are valid [col. 2, lines 40-43]; (f) arbitrating said valid commands [col. 3, lines 58-62]; (g) executing sequential valid commands of the same command type [col. 3, lines 24-25].

It would have been obvious to one of ordinary skill in the art, having the teachings of Stracovsky and Harriman before him at the time the invention was made, to modify the system of Stracovsky to include (e) determining if said reordered commands are valid; (f) arbitrating said valid commands (g) executing sequential valid commands of the same command type because it would have increased memory access efficiency by (1) improving overall locality of reference and/or command type and (2) balancing latency and bandwidth concerns as taught by Harriman.

As per claim 2, Stracovsky discloses said command types are forms of store and fetch commands [col. 12, line 58].

As per claim 3, Stracovsky discloses said command types are associated with a particular source or destination of said received memory commands [col. 7, lines 61- col. 8, line 26].

As per claim 4, Stracovsky discloses said particular source or destination is a particular computer processor connected on said bus [col. 6, lines 7-10].

As per claim 5, the concept of a particular source or destination being an I/O hub controller functionally connected on a bus is well known in the state of the art.

As per claim 6, the concept of a particular source or destination being a switching fabric connected to a bus is well known in the state of the art.

As per claim 7, the concept of a particular source or destination being a compression/decompression engine functionally connected to a bus is well known in the state of the art.

As per claim 8, Stracovsky discloses said command types which originate from or are required for a particular application have priority [col. 8, lines 30-33].

As per claim 9, Stracovsky discloses said step of receiving a plurality of commands further comprises determining if any of said received commands have an address dependency and passing said address dependency determination with said memory command [col. 6, lines 13-20].

As per claim 10, Stracovsky discloses said step of determining memory cycle performance penalties of said categorized commands further comprises comparing a number of oldest received categorized commands with each other [col. 20, lines 45-50].

As per claim 11, Stracovsky discloses said step of determining memory cycle performance penalties of said categorized commands further comprises comparing a number of oldest received categorized commands with a previously chosen command [col. 18, lines 1-7].

As per claim 12, Harriman discloses said step of determining memory cycle performance penalties of said categorized commands further comprises comparing a

number of oldest received categorized commands with a previously chosen command [col. 3, lines 60-62].

As per claim 13, Stracovsky discloses said step of reordering said categorized commands further comprises selecting the oldest of said categorized commands that have the least memory cycle performance penalty for execution [col. 20, lines 45-50].

As per claim 14, Harriman discloses said step of arbitrating said reordered valid commands further comprises granting priority to said type of command having said least memory cycle performance penalty [col. 4, lines 2-5].

As per claim 15, Harriman discloses said step of arbitrating said reordered valid commands further comprises granting priority to a command type other than said command type of said reordered valid commands [col. 7, lines 20-24].

As per claim 16, Harriman discloses said step of executing sequential valid commands of the same command type further continues a valid memory command of said command type is no longer available, or until a predetermined number has been executed, or until a memory command of another of said command types has higher priority [col. 3, lines 44-64].

Claim 17 is rejected as per claims 1, 2, 9-13 and 16 above.

Claim 18 is rejected as per claims 1 and 16 above.

Claim 21 is rejected as per claims 1, 11, 12, 13 and 16 above.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach reordering commands, determining command types, commands arbitration.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

  
MATTHEW KIM  
SUPERVISORY PATENT EXAMINER  
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*PMV*  
Pierre M. Vital  
September 30, 2002